# PHOTOGENIC

# D2.1

# Growth of VCSEL on Ge by MOCVD and MBE

| Project number: | 101069490 |
|---|---|
| Project acronym: | PhotoGeNIC |
| Project title: | Photonics on Germanium - New Industrial Consortium |
| Start date of the project: | 1st October, 2022 |
| Duration: | 36 months |
| Programme / Topic: | HORIZON-CL4-2021-DIGITAL-EMERGING-01-07 |

| Deliverable type: | DEM |
|---|---|
| Deliverable reference number: | ICT-07-824962 / D2.1/ V1.0 |
| Work package contributing to the deliverable: | WP2 |
| Due date: | October 2023 – M13 |
| Actual submission date: | 16th November, 2023 |

| Responsible organisation: | VIGO |
|---|---|
| Editor: | Wlodek Strupinski |
| Dissemination level: | PU |
| Revision: | 1.0 |

| Abstract: | This report constitutes summary on the technology development of Ge-VCSEL epitaxial heterostructure in comparison to GaAs-VCSEL growth. |
|---|---|
| Keywords: | Epitaxy, MOCVD, MBE, Growth |

## Editor

Wlodek Strupinski (VIGO)

## Contributors (ordered according to beneficiary numbers)

All partners

## Disclaimer

# Executive Summary

This deliverable aims to provide an update on the developments of the epitaxial technology of VCSEL heterostructure grown on Germanium substrates by MOCVD (MOVPE) and MBE techniques. The described activities in the period M01-M12 are related to WP2 for the Emerging technology for future VCSEL on Ge and depend on the activities on device processing within WP2 as the verification of the technology quality. The chapter 2 reports about the VCSEL designing and numerical analysis during MOCVD technology development. The chapter 3 reports the key items of MOCVD growth.
The deliverable enables the fabrication of the devices in WP3, the work progress in WP4 and after the devices fabrication it will enable works in WP5. It will enable also the comparison of MOCVD and MBE grown VCSELs.

# Table of Content

# List of Figures

# List of Tables

# Chapter 1    Introduction

The first campaign of development of the epitaxial growth of VCSEL structures on Ge substrates included several steps: VCSEL designing and simulation (TUL), production of N-type Ge bulk crystal and 4" wafers and delivery to VIGO (UMICORE), MOCVD epitaxy on GaAs and Ge, characterization of epi-stack GaAs-VCSEL and Ge-VCSEL at different phases of technology development (VIGO, LAAS, TUL). Processing and devices fabrication were performed within WP3 to give feedback on the laser performance which was used to plan next steps towards Ge-VCSEL epitaxy optimization. Due to serious machine technical issues the growth of Ge-VCSEL by MBE method (LAAS) is on delay and will be continued in the next months. However, it does not create a major risk for the project as the MBE method application is aiming at supporting research on MOCVD growth helping to understand the specificity of epitaxy on Ge substrates. It will be combined during the second Ge-VCSEL growth campaign aiming at further technology optimization.
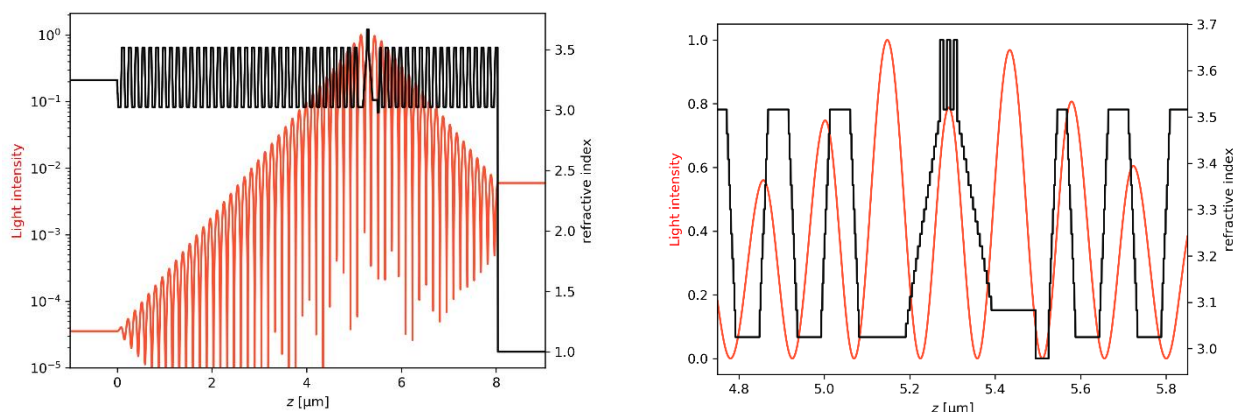
# Chapter 2     Design of VCSEL architecture

## 2.1  Designing of Ge-VCSEL epi-stack for 940nm wavelength

The works on the project began with the development of a design of the VCSEL epitaxial structure for 940nm emission as the most desirable in 3D camera and LIDAR applications. The theoretical design was developed by TUL and discussed by the entire consortium in terms of optimizing the required spectral parameters of the laser. The design process considered optimization with respect to stimulated emission efficiency (compositions and thicknesses of quantum wells and their number), the potential for achieving single-mode operation, and the reduction of optical absorption in the DBR mirrors and the cavity. Taking all these factors into account allowed us to propose designs specifying the thicknesses, mole fraction and doping levels of all layers.

*Table 1: Design of VCSEL 940nm to be grown on Ge substrate.*

**VCSEL 940 nm**

| Number | Material | repeat | thickness [nm] | Doping [cm$^{-3}$] | comments |
|---|---|---|---|---|---|
| 27 | GaAs | | 50 | p++ maximal | |
| 26 | Al$_{0.9}$Ga$_{0.1}$As -> GaAs | | 26.2 | p=2 10$^{18}$ | |
| 25 | Al$_{0.9}$Ga$_{0.1}$As | | 56.5 | p=2 10$^{18}$ | |
| 24 | GaAs -> Al$_{0.9}$Ga$_{0.1}$As | | 20 | p=2 10$^{18}$ | |
| 23 | GaAs | | 48.1 | p=2 10$^{18}$ | |
| 22 | Al$_{0.9}$Ga$_{0.1}$As -> GaAs | 17 | 20 | p=2 10$^{18}$ | |
| 21 | Al$_{0.9}$Ga$_{0.1}$As | | 56.5 | p=2 10$^{18}$ | |
| 20 | GaAs -> Al$_{0.9}$Ga$_{0.1}$As | | 20 | p=2 10$^{18}$ | |
| 19 | GaAs | | 22.9 | p=2 10$^{18}$ | |
| 18 | Al$_{0.8}$Ga$_{0.2}$As -> GaAs | | 20 | p=2 10$^{18}$ | |
| 17 | Al$_{0.98}$Ga$_{0.02}$As | | 30 | p=2 10$^{18}$ | to be oxidized |
| 16 | Al$_{0.8}$Ga$_{0.2}$As | | 104.0 | p=2 10$^{18}$ | |
| 15 | Al$_{0.4}$Ga$_{0.6}$As -> Al$_{0.8}$Ga$_{0.2}$As | | 40 | | |
| 14 | GaAs -> Al$_{0.4}$Ga$_{0.6}$As | | 40 | | |
| 10 | In$_{0.1}$Ga$_{0.9}$As | 2 | 7.5 | | |
| 9 | GaAs | | 10 | | active |
| 8 | In$_{0.1}$Ga$_{0.9}$As | | 7.5 | | |
| 10 | Al$_{0.45}$Ga$_{0.55}$As -> GaAs | | 40 | | |
| 9 | Al$_{0.9}$Ga$_{0.1}$As -> Al$_{0.45}$Ga$_{0.55}$As | | 40 | | |
| 8 | Al$_{0.9}$Ga$_{0.1}$As | | 109.8 | n=2 10$^{18}$ | |
| 7 | GaAs -> Al$_{0.9}$Ga$_{0.1}$As | | 20 | n=2 10$^{18}$ | |
| 6 | GaAs | 35 | 48.1 | n=2 10$^{18}$ | |
| 5 | Al$_{0.9}$Ga$_{0.1}$As -> GaAs | | 20 | n=2 10$^{18}$ | |
| 4 | Al$_{0.9}$Ga$_{0.1}$As | | 56.5 | n=2 10$^{18}$ | |
| 3 | Al$_{0.5}$Ga$_{0.5}$As -> Al$_{0.9}$Ga$_{0.1}$As | | 20 | n=2 10$^{18}$ | |
| 2 | Al$_{0.5}$Ga$_{0.5}$As | | 400 | n=2 10$^{18}$ | |
| 1 | GaAs | | 100 | n=4 10$^{18}$ | |
| 0 | Ge | | substrate | | |

1λ cavity
3x $In_{0.1}Ga_{0.9}As$ QWs
17 pair top $Al_{0.9}Ga_{0.1}As$/GaAs DBR
35 pair bottom $Al_{0.9}Ga_{0.1}As$/GaAs DBR

Designed wavelength 940 nm
Q-factor ~9200

*Figure 1: Simulation of the 940nm design.*

## 2.2 Numerical analysis loop

Based on reflectance measurements from wafers grown at VIGO after each growth process, a numerical analysis of the reflection spectra was performed. This involved aligning the experimental and numerical spectra, enabling the identification of any discrepancies in layer thicknesses and compositions relative to the initial designs. Multiple iterations of adjustments between measurements and numerical analysis led to achieving the expected parameters of wafers.

One of simulation examples (Figure 2) supported the technology of DBRs growth indicating the more important role of precise layers thickness control over Al content:

AlGaAs thickness change of 0.3% moves the DBR by 1nm
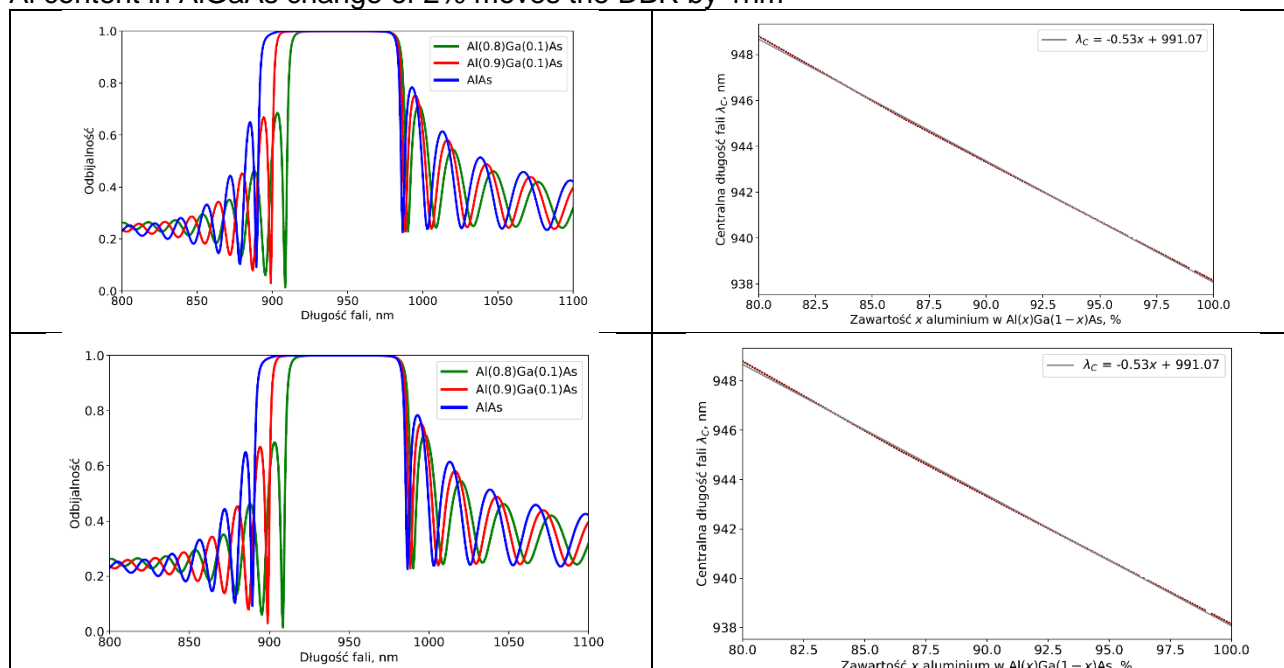Al content in AlGaAs change of 2% moves the DBR by 1nm



*Figure 2: Analysis of influence of Al content and layer thickness on DBR spectral position*

# Chapter 3    MOCVD growth of VCSEL heterostructure on GaAs and Ge substrates

.

*Table 2: Main blocks of VCSEL epi-stack.*

| Number | Material | repeat | thickness [nm] | Doping [cm$^{-3}$] | comments |
|---|---|---|---|---|---|
| 27 | GaAs | | 50 | p++ maximal | |
| 26 | Al$_{0.9}$ Ga$_{0.1}$As -> GaAs | | 26.2 | p=2 10$^{18}$ | |
| 25 | Al$_{0.9}$ Ga$_{0.1}$As | | 56.5 | p=2 10$^{18}$ | |
| 24 | GaAs -> Al$_{0.9}$ Ga$_{0.1}$As | | 20 | p=2 10$^{18}$ | |
| 23 | GaAs | | 48.1 | p=2 10$^{18}$ | |
| 22 | Al$_{0.9}$ Ga$_{0.1}$As -> GaAs | 17 | 20 | p=2 10$^{18}$ | |
| 21 | Al$_{0.9}$ Ga$_{0.1}$As | | 56.5 | p=2 10$^{18}$ | |
| 20 | GaAs -> Al$_{0.9}$ Ga$_{0.1}$As | | 20 | p=2 10$^{18}$ | |
| 19 | GaAs | | 22.9 | p=2 10$^{18}$ | |
| 18 | Al$_{0.8}$ Ga$_{0.2}$As -> GaAs | | 20 | p=2 10$^{18}$ | |
| 17 | Al$_{0.98}$ Ga$_{0.02}$As | | 30 | p=2 10$^{18}$ | to be oxidized |
| 16 | Al$_{0.8}$ Ga$_{0.2}$As | | 104.0 | p=2 10$^{18}$ | |
| 15 | Al$_{0.4}$Ga$_{0.6}$As -> Al$_{0.8}$ Ga$_{0.2}$As | | 40 | | |
| 14 | GaAs -> Al$_{0.4}$Ga$_{0.6}$As | | 40 | | |
| 10 | In$_{0.1}$Ga$_{0.9}$As | 2 | 7.5 | | |
| 9 | GaAs | | 10 | | active |
| 8 | In$_{0.1}$Ga$_{0.9}$As | | 7.5 | | |
| 10 | Al$_{0.45}$ Ga$_{0.55}$As -> GaAs | | 40 | | |
| 9 | Al$_{0.9}$ Ga$_{0.1}$As -> Al$_{0.45}$ Ga$_{0.55}$As | | 40 | | |
| 8 | Al$_{0.9}$ Ga$_{0.1}$As | | 109.8 | n=2 10$^{18}$ | |
| 7 | GaAs -> Al$_{0.9}$ Ga$_{0.1}$As | | 20 | n=2 10$^{18}$ | |
| 6 | GaAs | 35 | 48.1 | n=2 10$^{18}$ | |
| 5 | Al$_{0.9}$ Ga$_{0.1}$As -> GaAs | | 20 | n=2 10$^{18}$ | |
| 4 | Al$_{0.9}$ Ga$_{0.1}$As | | 56.5 | n=2 10$^{18}$ | |
| 3 | Al$_{0.5}$Ga$_{0.5}$As -> Al$_{0.9}$ Ga$_{0.1}$As | | 20 | n=2 10$^{18}$ | |
| 2 | Al$_{0.5}$Ga$_{0.5}$As | | 400 | n=2 10$^{18}$ | |
| 1 | GaAs | | 100 | n=4 10$^{18}$ | |
| 0 | Ge | | substrate | | |

DBR TOP (rows 20–23)

Oxidation layer Al$_{0.98}$GaAs (row 17)

MQWs (rows 8–10)

DBR BOTTOM (rows 4–7)

Epitaxy of VCSEL epi-stack by MOCVD (MOVPE) technique was developed. Systematic research on the growth of the main heterostructure blocks was performed first using GaAs substrates 4" diameter and then implemented into Ge wafers. The first design to work on was for 940nm of the wavelength (WL). Bottom Bragg reflectors, active region (AR), oxidation layer, top Bragg reflectors and cap contact layer were carefully optimized on GaAs to get the required spectral properties. Different PL's WL and the WL of the optical cavity required the gain peak to be offset from cavity resonance spectral position. Same methodology were applied for the VCSEL structure grown on Ge preceded by development of the special GaAs nucleation layer and Al0.5GaAs buffer layer growth conditions. In both cases (4" GaAs and 4" Ge) the final identical VCSEL heterostructures were produced and used for device processing.

Ge substrates 4" N-type were produced and delivered by UMICORE. Wafer specification for VCSEL growth are largely unknown. A first point to tackle is the wafer resistivity type and range. While p-type Ge crystals can be grown in a broad resistivity range, this is not the case for n-type, today the preferred resistivity type for VCSELs. Especially the high doping concentrations to reach ultra-low resistivities needed to overcome the Ge n-type contacting hurdle, is set to be challenging.

The template wafers for MBE growth, i.e. 4" Ge wafers covered with GaAs nucleation and Al0.5GaAs buffer layers were fabricated. The wafers were characterised prior to the MBE growth by AFM and XRD.

The GaAs nucleation layer is crucial for the entire Ge-VCSEL heterostructure's crystallographic quality. Special attention was devoted to analyse the MOCVD growth conditions of this nucleation layer, in particular to its surface morphology, i.e. roughness measured by Atomic Force Microscopy. The achievement of the roughness (Ra) below 1nm enabled further technological works on the subsequent AlGaAs buffer layer optimization and the whole VCSEL epi-stack. The grown Al0.5GaAs 500nm thick buffer of a good morphology was well lattice matched to Ge substrate which was confirmed by XRD measurements. The lattice mismatch of the GaAs and AlGaAs layers creating the VCSEL structure grown on the Al0.5GaAs buffer is twice lower than the lattice mismatch between GaAs substrate and Al0.9GaAs. This solution ensured a reduction in the density of misfit defects which improved spectral quality of the device.
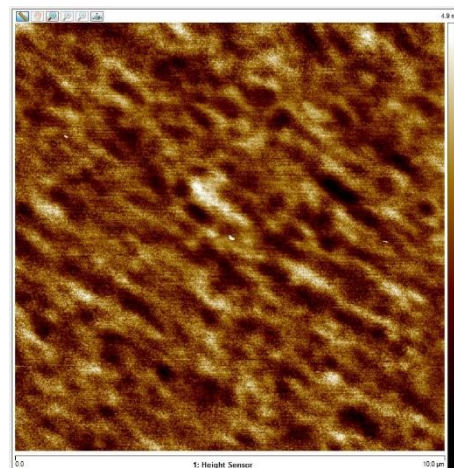


*Figure 3: AFM image of GaAs/Al$_{0.5}$GaAs nucleation/buffer layers grown on Ge substrate. RMS = 0.7nm*

## 3.1 Development of doping and AlGaAs composition

The systematic calibration of the required Al content in Al$_x$Ga$_{1-x}$As layers was performed in a wide range for x=0-1. Doping was optimized in relation to the AlGaAs chemical composition and the growth rate. Silane as the silicon precursor was used for N- type doping and CBr$_4$ as carbon source for P-type. Hall and ECV methods were used for measurement of carrier concentration, verified additionally by SIMS. The reaction of CBr$_4$ with Aluminium in the reactor was analysed and Al-content correctios were introduced in AlGaAs:C layers. AlGaAs composition was estimated by photoluminescence and XRD methods for direct E$_g$ and by XRD for indirect band gap (x>0.43). Several test Bragg reflector structures doped at different level with Si and C were produced in order to measure and optimize layers resistivity independently of theoretical predictions and concentration measurements. AlGaAs composition and its thickness was also controlled during the growth by reflectance in-situ technique.
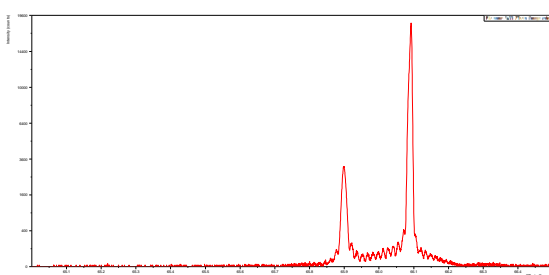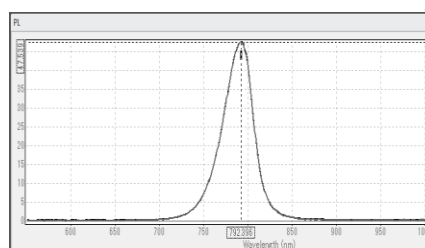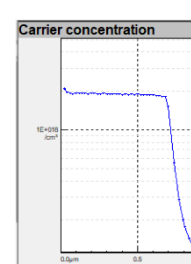


(a)  (b)  (c)

*Figure 4: Example of XRD spectrum (a) and PL peak (b) to estimate Al content in AlGaAs compound and ECV profile of electron concentration (c).*
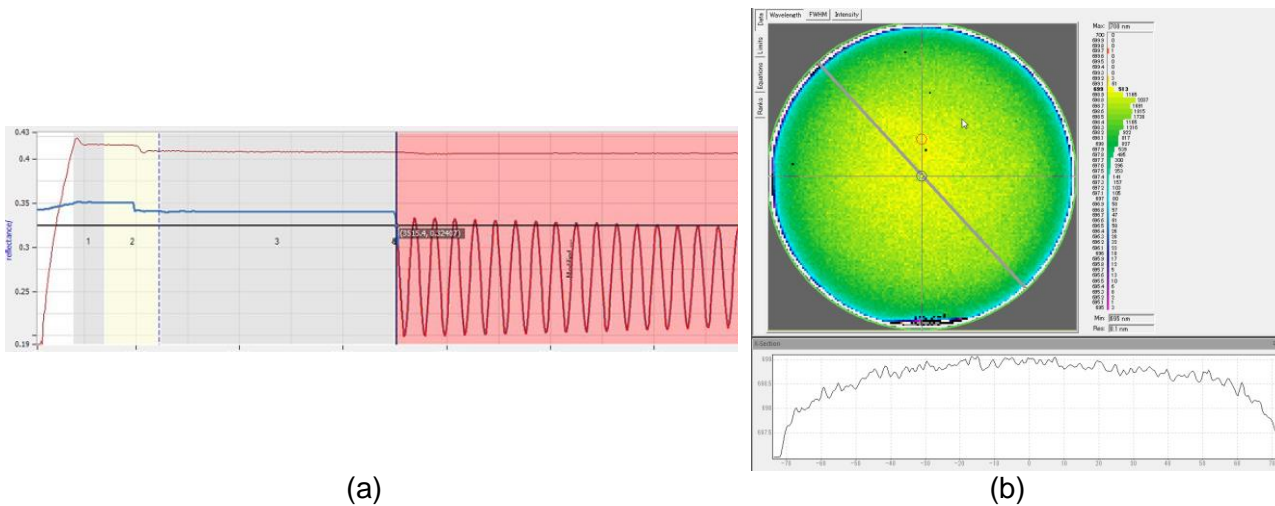
(a)                                                                 (b)

*Figure 5: Reflectance in-situ results of AlGaAs composition and thickness (a), PL map of Al$_{0.3}$GaAs grown on Ge 6" substrate (P-type in this case).*

## 3.2 Growth of DBRs

Bottom and top DBR were developed in the same way both for GaAs and Ge substrates. The characterization was based on reflectance method in-situ and ex-situ. Technology optimization was aimed at obtaining the flat plateau within circa 100nm wide and DBR centre at 940nm. Figure 6 presents the evolution of DBR optimization supported by theoretical simulations made at TUL (Figure 7).
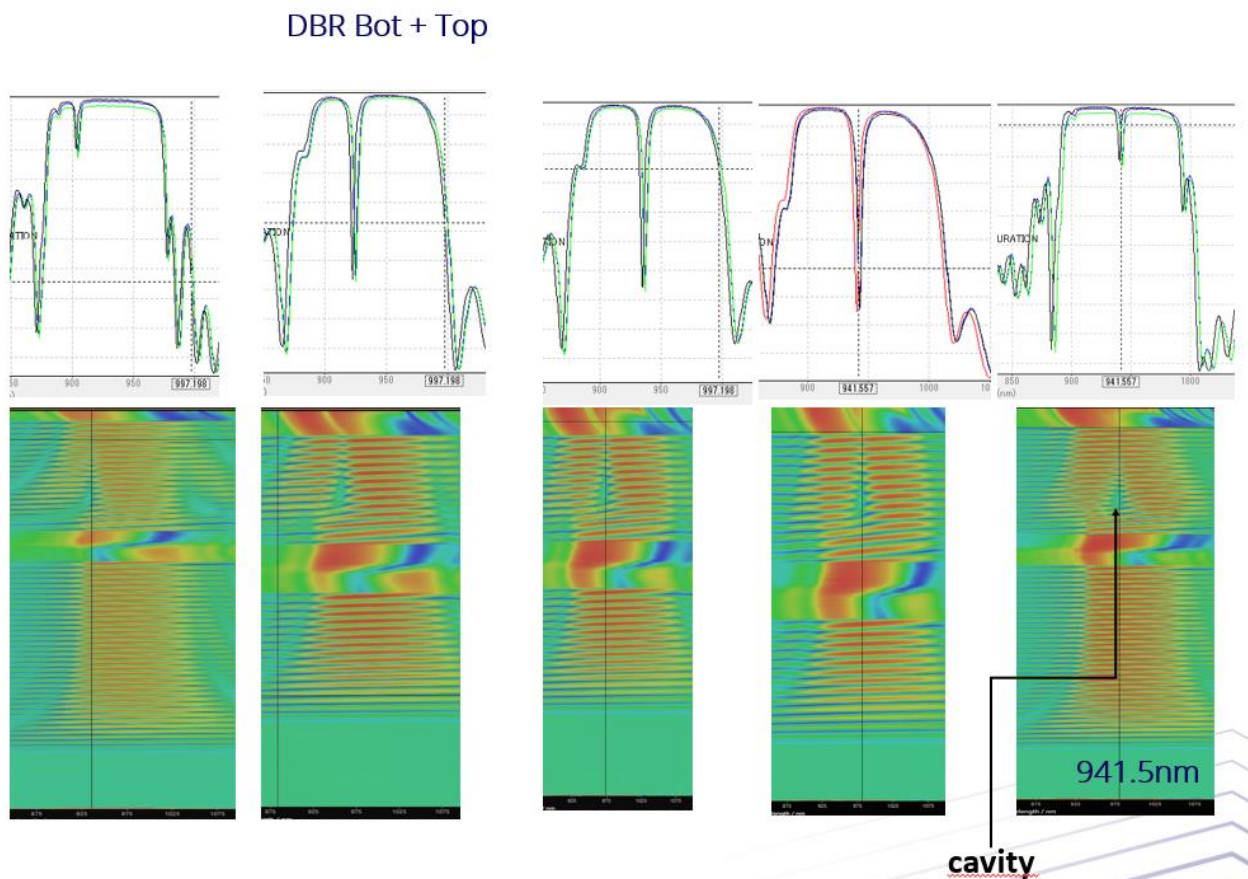


*Figure 6: Reflectance ex-situ (top raw) and in-situ (bottom raw) of DBR growth optimized by adjusting layers thickness.*
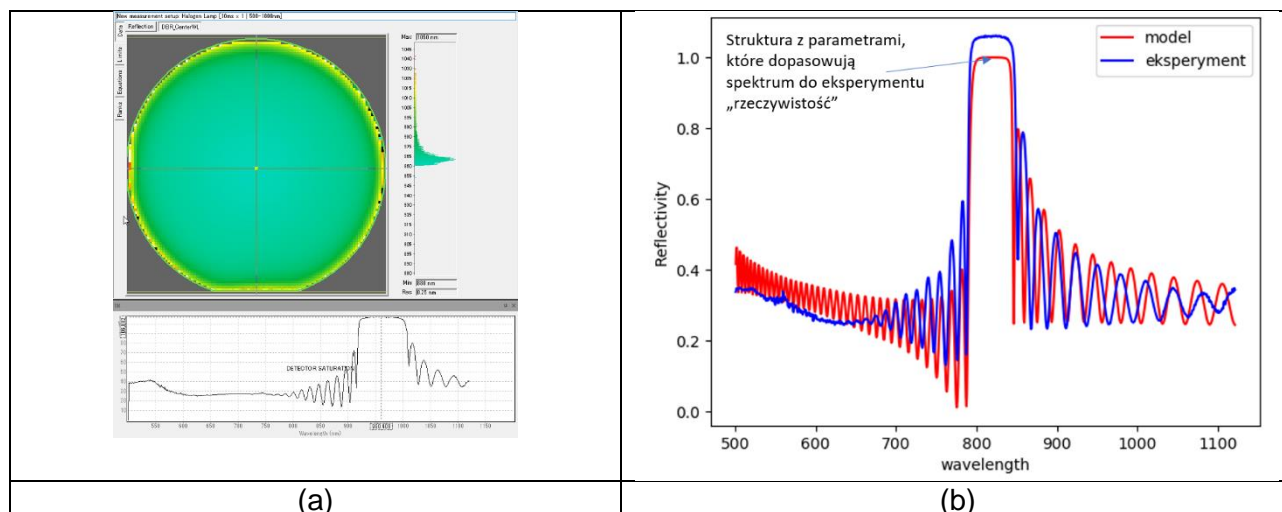
| (a) | (b) |

*Figure 7: (a) reflectance map of DBR with the centre at 940nm, (b) theoretical prediction for layer thickness tuning.*

## 3.3  Development of MQW

$In_{0.16}GaAs$ compound was designed as the quantum well in the VCSEL structure. The growth development was based on the measurements using X-ray diffraction to achieve the required QW composition and PL mapper to adjust the wavelength precisely. The wavelength and uniformity across the wafer were examined and calibrated.
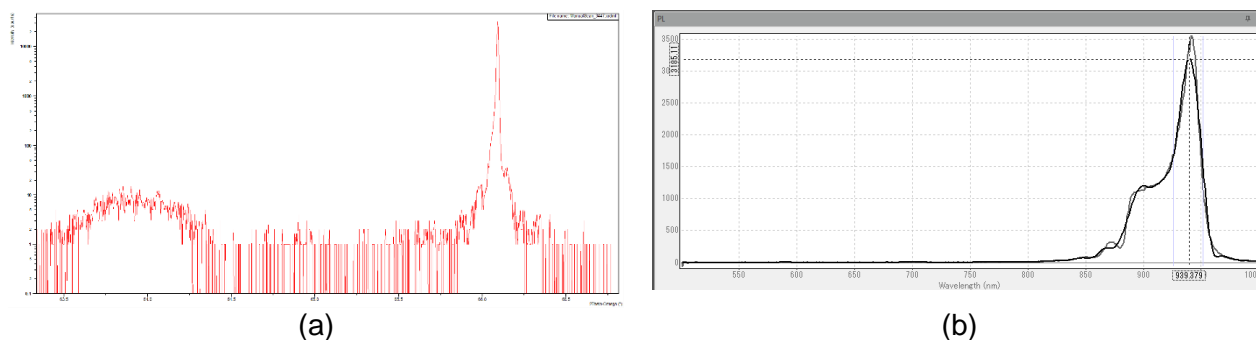


| (a) | (b) |

*Figure 8: (a) XRD spectrum of InGaAs strained layer with In content = 0.16; (b) PL of InGaAs QW (940nm)*

In order to better estimate QW thickness the super-lattice structure InGaAs/GaAs was grown and analysed by XRD measurements.
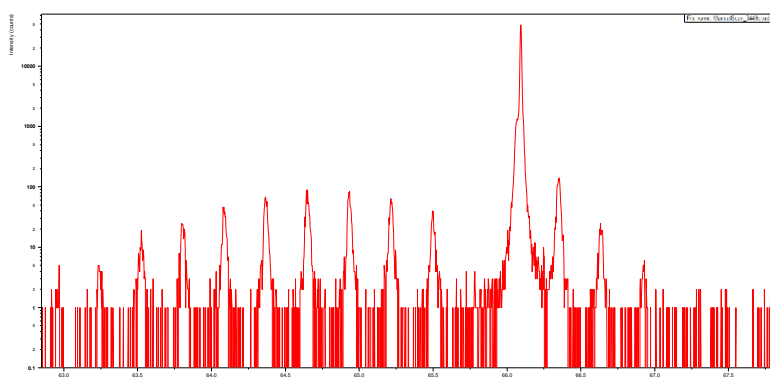


*Figure 9: $In_{0.16}GaAs/GaAs$ super-lattice XRD spectrum.*

## 3.4 Growth of entire VCSEL structure

The growth of the entire VCSEL structure was performed first using GaAs substrates 4" diameter and then implemented into Ge wafers, both for 940nm of the wavelength (WL). Bottom Bragg reflectors, active region (AR), oxidation layer, top Bragg reflectors and cap contact layer were carefully optimized on GaAs to get the required spectral properties. Different PL's WL and the WL of the optical cavity required the gain peak to be offset from cavity resonance spectral position. Same methodology were applied for the VCSEL structure grown on Ge preceded by development of the special GaAs nucleation layer and Al0.5GaAs buffer layer growth conditions. In both cases (4" GaAs and 4" Ge) the final identical VCSEL heterostructures were produced and used for device processing within the WP3. All characterization results of the material and measurement results of the devices creates a data base for further Ge-VCSEL technology optimization.
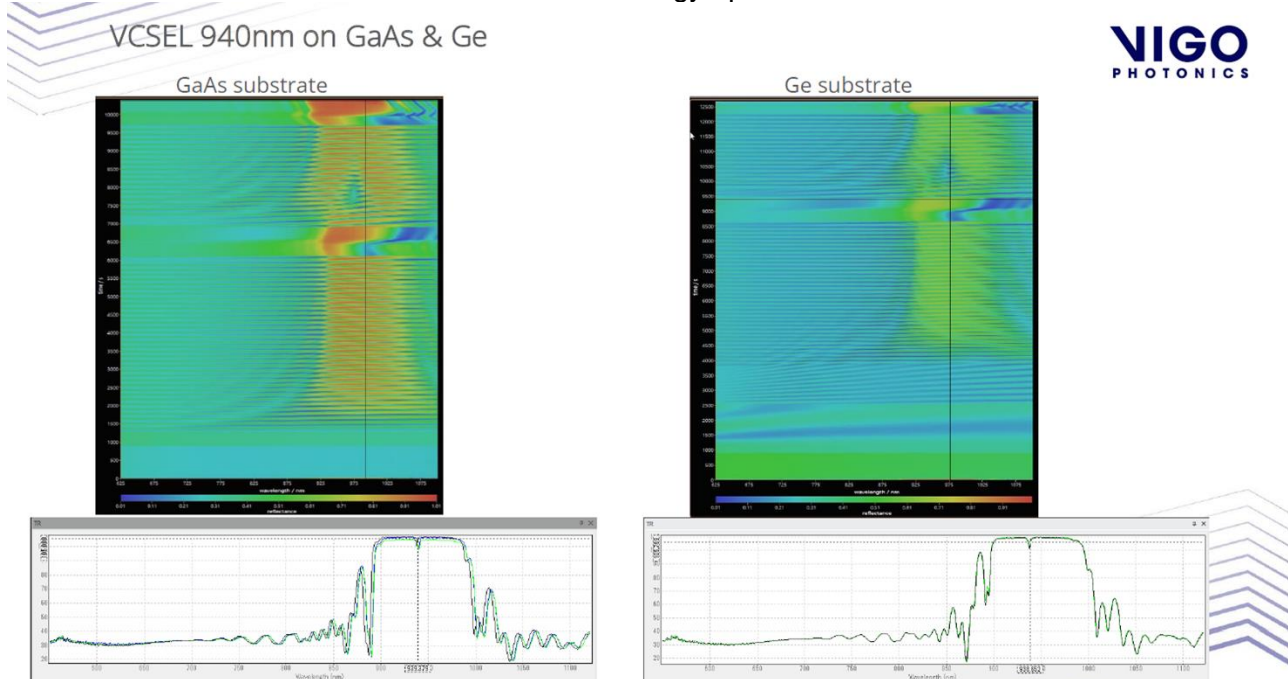


*Figure 10: In-situ and ex-situ reflectance measurement results of VCSEL structure grown on GaAs and Ge substrates.*
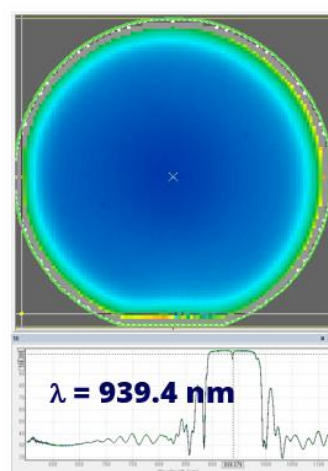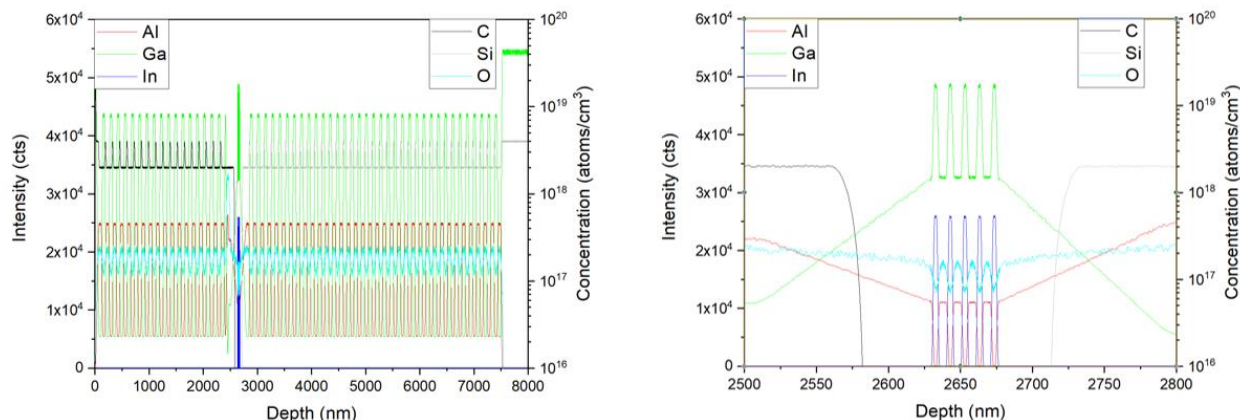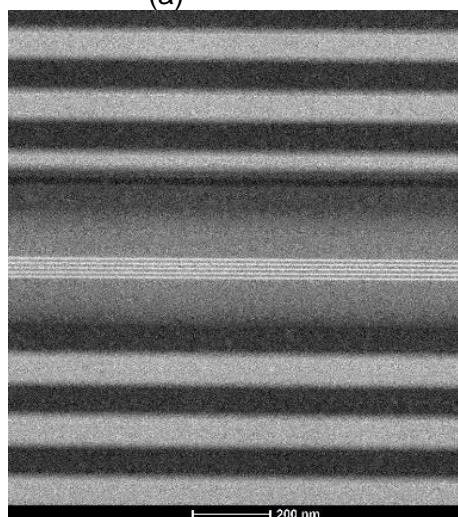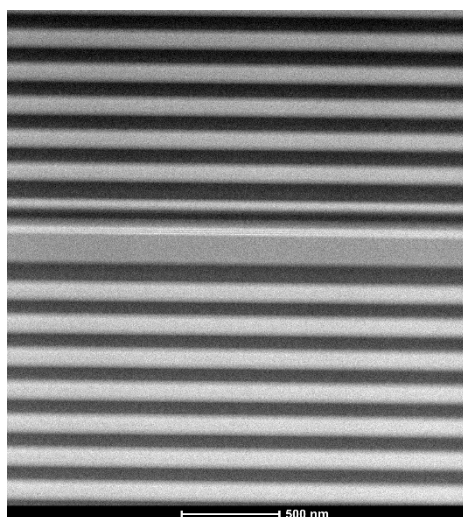


*Figure 11: Reflectance map shows good uniformity of the dip spectral position (matter for further improvement).*

SIMS using high depth resolution tool, SEM and TEM measurements confirmed good quality and repeatability of the VCSEL's layers.



(a)



(b)

*Figure 12: (a) SIMS measurement results of VCSEL structure with the profiles of dopants Si, C and oxygen impurity; (b) TEM images of the active region and DBRs.*

The preliminary observations of lower bow parameter in case of Ge-VCSEL in comparison to GaAs-VCSEL epi-structure was confirmed by deflectometry measurements performed at LAAS-CNRS. GaAs/AlGaAs VCSELs are compressively stressed on GaAs but strain-balanced on Ge
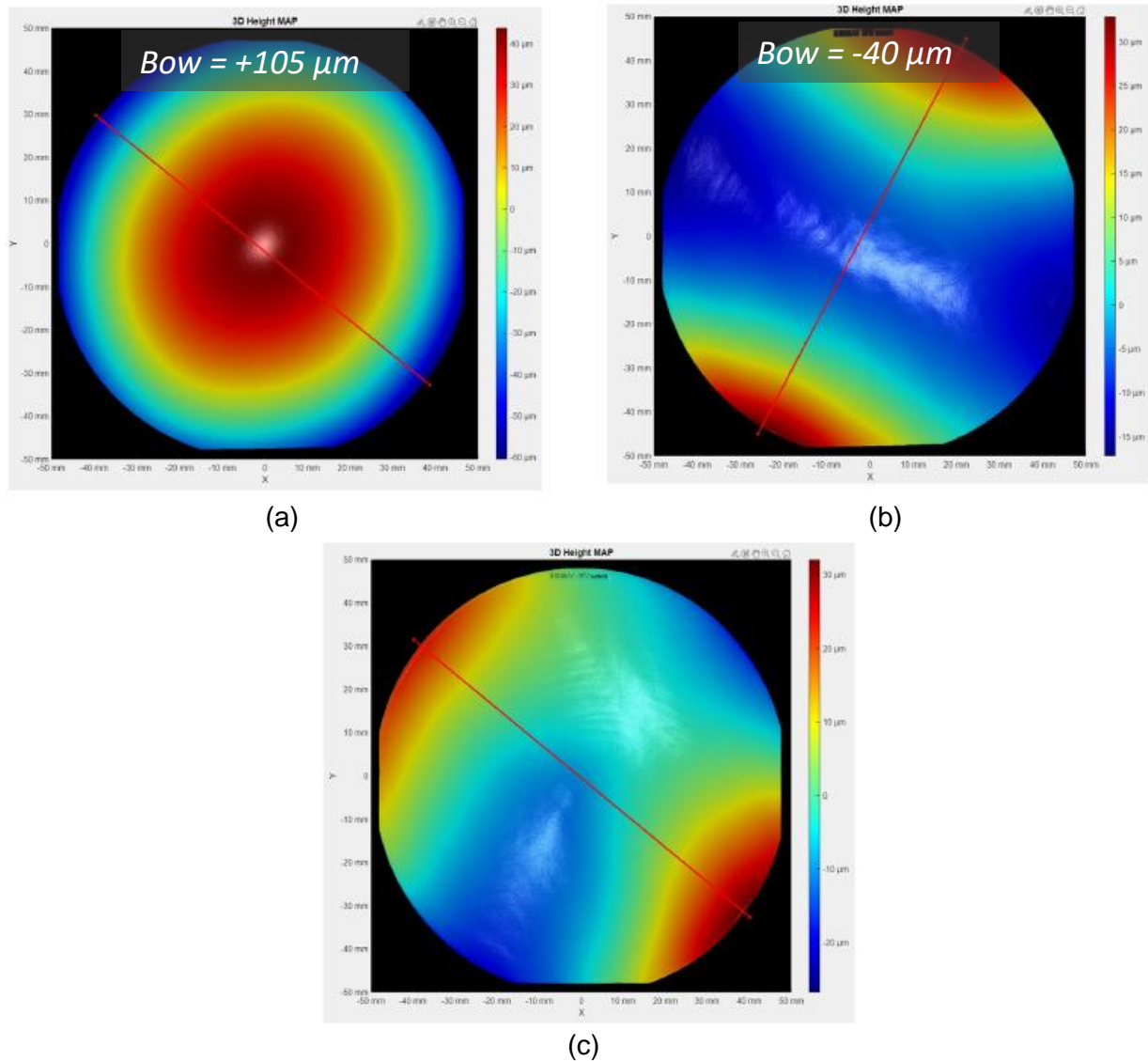
(a)



(b)



(c)

*Figure 13: (a) VCSEL on 4'' GaAs; (b) VCSEL on 4'' Ge; (c) no visible bow in case of GaAs/Al$_{0.5}$GaAs buffer on Ge*

Oxidation of Al$_{0.98}$GaAs performed in test samples and processed wafers (mesas) confirmed proper aperture thickness as designed and uniform. This will be further investigated (Figure 14).
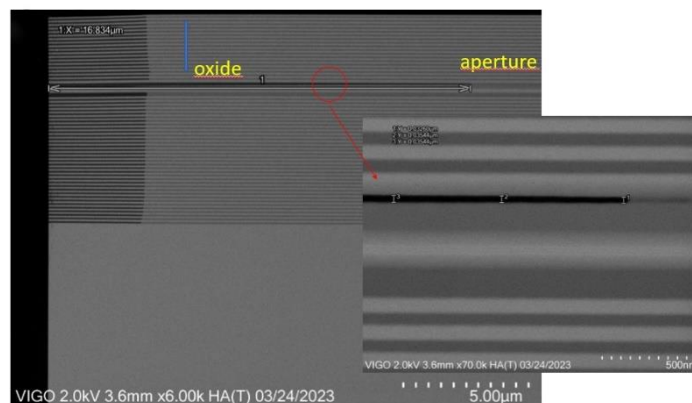


*Figure 14: Ge-VCSEL after oxidation of Al$_{0.98}$GaAs layer.*

# Chapter 4    Summary and Conclusion

Ge-VCSEL epi-structure growth by MOCVD (MOVPE) method was successfully developed. The first 4" epi-wafers were produced, characterized and delivered to the WP3 for devices processing. Epi quality was confirmed by the fast and preliminary processing realized by the consortium partner – pmd. The first Ge-VCSEL devices were produced and the results were reported during the conference VCSEL Day in Torino (Oct.2023). Full process flow is to be finished soon by the consortium partner – IMiF. Obtained results will be analysed in comparison to GaAs-VCSEL produced parallelly and used for optimization of epitaxial growth in the next campaign.

Achieved results confirmed the proper growth conditions of the AlGaAs buffer on Ge enabling the growth of the entire VCSEL epi-stack. The templates – Ge wafers with the buffer were produced and will be used in VCSEL growth by MBE technique.

The wafer bow is significantly lower than in case of GaAs. Consumption of arsine was reduced. The Ge substrates quality and resistivity is optimal.

The works in next steps of the WP2 will focus on optimization of the epi-structure design, on further improvement of structural quality of the layers grown on Ge and on studies of uniformity and repeatability.
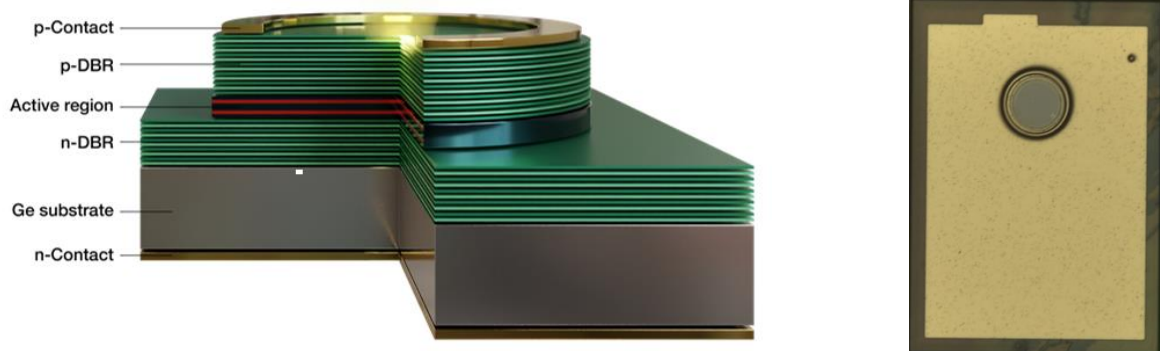


*Figure 15: Ge-VCSEL*